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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,361	07/30/2001	Steven C. Woo	RB1-026US	2536

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EXAMINER	
VERBRUGGE, KEVIN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,361	WOO ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,24-26,28-35,38-40 and 52-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25,26,28-35,52,53,55-57 and 59-67* is/are allowed.

6)☒ Claim(s) *1-21,24,38-40,54 and 58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/26/05 has been entered.

Response to Amendment

This non-final Office action is in response to the RCE mentioned above and the amendment submitted 1/26/05 which amended several claims. Claims 1-21, 24-26, 28-35, 38-40, and 52-67 are pending. All objections and rejections not repeated below are withdrawn. Applicant's arguments are addressed following the rejections.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 11, 19, and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear what is meant by the phrase "on a same device as the memory cells" in the last two lines of the claim 19 (and "other device" or "different device" language in the other claims). It had been clear that "same device" meant the logical unit holding the memory cells, but Applicant has attempted to recharacterize this phrase in the response filed 1/26/05 creating uncertainty in the term's meaning.

In the claim, the phrase "on a same device as the memory cells" apparently refers to the memory device of line 2 in the claim.

In the specification, the Applicant shows memory devices 16 and in use registers 24 in Figs. 1, 2, 4, 5, 6, and 8. In Figs. 2, 5, 6, and 8, the in use registers 24 are clearly shown located on the same memory device 16 as the memory cells 22, while in Figs. 1 and 4, the in use registers 24 are clearly shown separate from memory devices 16 (in Fig. 1 the in use registers 24 are in a standalone unit connected to the memory controller 14 while in Fig. 4, the in use registers 24 are shown inside memory controller 14.

Clearly then, Applicant has explicitly shown multiple embodiments where the in use registers 24 are not implemented on a same memory device as the memory cells (see Figs. 1 and 4). Again, the "same device" of claim 19, next to last line, is understood to mean "same memory device", referring to the memory devices of line 2, since this is the only device mentioned in the claim.

The difficulty arises due to the recharacterization of the term device as presented in the amendment above where Applicant is attempting to characterize the term "device"

to mean "integrated circuit" or "chip" to overcome the Boyer reference which Applicant asserts discloses only a single chip having all functional units combined thereon.

Therefore, it is no longer clear what is meant by the claim term "device". The public cannot ascertain whether it means the unit holding the memory cells as shown in Figs. 1, 2, 4, 5, 6 and 8 and mentioned at page 3, line 11, of the specification, or whether it means an entire integrated circuit chip which contains the memory cells and other functional units.

The meaning of "device" is further clouded by the specification's teaching that the memory devices can be integrated in the CPU and/or the memory controller at page 3, lines 3-6. Is Applicant now disclaiming this embodiment of the invention?

Finally, the specification also uses the word "device" to refer to entire systems made of many chips (see page 3, lines 15-19, for example). Presumably the Applicant is not intending to claim an invention where the use registers are implemented in an altogether separate system, but due to the uncertainty created by the Applicant's remarks, one cannot be sure.

Therefore the 112 2nd rejection is made to require correction of the now uncertain phrase "on a same device as the memory cells".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7-16, 18, 19, 20, 24, 38, 39, 54, and 58 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,167,484 to Boyer et al.

Regarding claims 19 and 20, Boyer shows the claimed one or more memory devices as memory array tiles 802 in Fig. 8.

Boyer shows the claimed memory controller as system DRAM controller 820 in Fig. 8, for example (a similar circuit is shown in Fig. 9).

He does not explicitly show the claimed refresh logic to refresh the memory cells, however the claimed refresh logic is inherent in his device and its presence in system DRAM controller 820 is indicated by the refresh signal REF leaving controller 820.

He shows the claimed dynamically changeable use registers as tile history qualifiers 808a, 808b, ... 808N. These qualifiers correspond to groups of one or more memory cells, as claimed, and indicate whether the corresponding groups of memory cells are in use (column 5, lines 11-14, column 8, lines 1-3, column 14, line 48 through

column 15, line 36, column 24, lines 40-43, column 25, line 50 through column 26, line 25).

Boyer's refresh logic omits refreshing of memory cells that are not in use as claimed (column 5, lines 14-19, column 7, lines 46-51).

Boyer's history qualifiers anticipate the claimed recent-access flags, since his history qualifiers are "processed whereby refreshing is not performed on a row of cells that do not need refreshing (i.e., rows that are inactive, or rows that were recently read or written since these accesses inherently do a refresh of the rows)" (emphasis added, column 5, lines 16-19). Boyer clearly teaches that one of the key advantages of his device is keeping track of reads and writes with his history qualifier bits so that memory locations which have recently been read or written (which inherently performs a refresh of the accessed location) are not needlessly refreshed soon after, wasting power and processing time and bandwidth (column 3, lines 22-28). Other passages addressing this key advantage of his device include column 7, lines 12-18 and 46-51, column 14, lines 38-48, and column 23, lines 3-8.

Boyer's history qualifiers are not implemented on a same device as the memory array tiles. They are clearly part of a separate functional unit (history decoder 804), entirely separate from memory array tiles 802. Boyer anticipates the claimed invention even if Boyer's system is on a single chip. The broadest reasonable interpretation of "device" is a functional unit, separate and distinct from other functional units.

Clearly the history decoder 804 is separate from memory array tiles 802. Integration of plural devices (such as a CPU, system DRAM controller, history decoder,

and memory array tiles) onto a single chip does not remove the distinction between the devices. The broadest reasonable interpretation of the word "device" includes different elements of a single integrated chip. Particularly relevant passages of Boyer are found at column 14, lines 53-56 and column 15, lines 22-25 where he teaches that history decoder 804 is a "stand alone" unit "separate from the memory array tiles 802."

A particularly relevant passage of the specification is page 3, lines 3-6, where Applicant teaches that "Although the memory controller and memory devices are shown to be separate entities in this figure [Fig. 1], the same techniques apply for memory controllers that are integrated into the CPU, as well as memory that is integrated with either the controller and/or the CPU."

Any subsequent attempt by Applicant to assert that the Examiner's position that Boyer's use registers are not on the same device as the memory cells must address all of these issues and clearly define the term "device," particularly as it relates to distinct elements on a single chip and provide support from the specification for such a definition, if that is possible. Until such time, the Examiner's interpretation of "device" (as in claim 19 for example) as anticipated by separate units on a single chip will stand as reasonable.

Regarding claim 24, Boyer variously describes his history qualifiers as referring to rows, refresh groups, pages (column 5, line 13, column 8, line 2, column 10, lines 62-67, column 24, lines 41-43, and column 25, line 65).

Regarding claims 1, 2, 11, 12, 38 and 54, Boyer shows the claimed memory controller as system DRAM controller 820 and history decoder 804 in Fig. 8, for example (a similar circuit is shown in Fig. 9). It is entirely appropriate to consider these two elements together as making up the claimed memory controller since both elements function together to control memory array tiles 802.

He does not explicitly show the claimed refresh logic to refresh the memory cells, however the claimed refresh logic is inherent in his device and its presence in system DRAM controller 820 is indicated by the refresh signal REF leaving controller 820.

He shows the claimed dynamically changeable use registers as tile history qualifiers 808a, 808b, ... 808N. These qualifiers correspond to groups of one or more memory cells, as claimed, and indicate whether the corresponding groups of memory cells are in use (column 5, lines 11-14, column 8, lines 1-3, column 14, line 48 through column 15, line 36, column 24, lines 40-43, column 25, line 50 through column 26, line 25).

Boyer's refresh logic omits refreshing of memory cells that are not in use as claimed (column 5, lines 14-19, column 7, lines 46-51).

Boyer's memory controller (shown as DRAM controller 820 and history decoder 804) is a device other than the memory device as claimed. Boyer's memory controller is separate and distinct from his memory array tiles, even if all of Boyer's elements are located on a single chip. The broadest reasonable interpretation of the term "device" allows for the characterization of the memory array tiles of Boyer to be separate devices

from the other devices on his chip. Further explanation is found above in the grounds of rejection of claim 19 and below in the response to arguments regarding claim 19.

Regarding claims 3, 13, 15, 39, and 58, Boyer's history qualifiers anticipate the claimed recent-access flags, since his history qualifiers are "processed whereby refreshing is not performed on a row of cells that do not need refreshing (i.e., rows that are inactive, or rows that were recently read or written since these accesses inherently do a refresh of the rows)" (emphasis added, column 5, lines 16-19). Boyer clearly teaches that one of the key advantages of his device is keeping track of reads and writes with his history qualifier bits so that memory locations which have recently been read or written (which inherently performs a refresh of the accessed location) are not needlessly refreshed soon after, wasting power and processing time and bandwidth (column 3, lines 22-28). Other passages addressing this key advantage of his device include column 7, lines 12-18 and 46-51, column 14, lines 38-48, and column 23, lines 3-8.

Regarding claim 4, Boyer shows plural memory devices in Fig. 8.

Regarding claims 5 and 14, Boyer shows a memory device including the history qualifiers in Fig. 2. In column 14, lines 50-56, he teaches that "the memory system 200 of Fig. 2 ... has history bits located locally within the various memory blocks/tiles and usually in line with the memory row decoder".

Regarding claims 7-10 and 18, Boyer variously describes his history qualifiers as referring to rows, refresh groups, pages (column 5, line 13, column 8, line 2, column 10, lines 62-67, column 24, lines 41-43, and column 25, line 65).

Regarding claim 16, unused memory cells that are not refreshed, as in Boyer's device, are operated at reduced power as claimed (see column 25, lines 60-61 as claimed).

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 17, 21 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al. in view of U.S. Patent 5,265,231 to Nuwayser further in view of Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Boyer does not disclose a cache in his memory controller.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a cache in Boyer's memory controller for the improved operation speed provided by a cache as known in the art at the time of the invention. Furthermore, as taught by Ohsawa, data that is cached in the memory controller need not be refreshed in the memory as long as it is eventually written back to the memory.

Response to Arguments

Applicant's arguments have been considered but they are not persuasive.

Regarding claim 19, on page 22 of the amendment, last paragraph, Applicant argues that Boyer teaches that his components are located "on a single device," "in an embedded DRAM device," an in "an embedded DRAM integrated circuit." It is understood from this discussion that Applicant is asserting that Boyer's invention has all components on a single integrated circuit chip.

Even if it is true that Boyer's system is all on a single chip, the broadest reasonable interpretation of the term "device" in claim 19, next to last line, is that a device is a functional unit, separate and distinct from other functional units. While this definition includes chips, it also includes functional units on chips as in Boyer. So while a particular interpretation of Boyer's chip may characterize it as a device, an equally proper characterization of the term "device" is reasonably applied to the separate and

distinct functional units within a chip. No definition of the term "device" in the specification or in the art requires otherwise.

Integration of plural devices (such as a CPU, system DRAM controller, history decoder, and memory array tiles) onto a single chip does not necessarily remove the distinction between the devices. The broadest reasonable interpretation of the word device includes different elements of a single integrated chip.

Boyer clearly shows his history decoder 804 (which contains history qualifiers 808) separate and distinct from his memory array tiles 802, therefore his history decoder is properly considered a separate device from the memory tile arrays. Particularly relevant passages of Boyer are found at column 14, lines 53-56 and column 15, lines 22-25 where he teaches that history decoder 804 is a "stand alone" unit "separate from the memory array tiles 802."

It is not reasonable to equate the claim term "device" with "integrated circuit chip" as Applicant is attempting to do, particularly in light of the lack of such a definition presented in the specification and the lack of such a definition in the art. Furthermore, at page 3, lines 3-6, of the specification, Applicant teaches that "Although the memory controller and memory devices are shown to be separate entities in this figure [Fig. 1], the same techniques apply for memory controllers that are integrated into the CPU, as well as memory that is integrated with either the controller and/or the CPU" further clouding the issue.

Any subsequent attempt by Applicant to assert that the Examiner's position that Boyer's use registers are not on the same device as the memory cells must address all

of these issues and clearly define the term "device," particularly as it relates to distinct elements on a single chip and provide support from the specification for such a definition, if that is possible. Until such time, the Examiner's interpretation of "device" (as in claim 19 for example) as anticipated by separate units on a single chip will stand as reasonable.

Regarding claims 1, 11, and 38, Applicant's arguments have been considered but are moot in view of the new grounds of rejection.

Regarding claims 25, 52, 61, and 65, Applicant's arguments have been considered and are persuasive.

Regarding claim 32, the amendments overcome the rejection.

Allowable Subject Matter

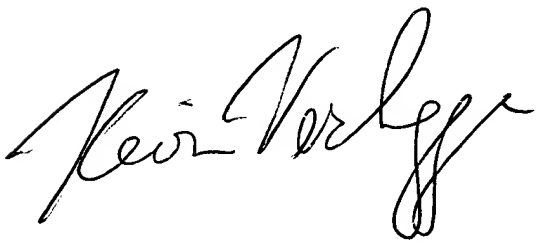
Claims 25, 26, 28-35, 52, 53, 55-57, and 59-67 are allowed.

Conclusion

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (571) 272-4214.

Any response to this action should be labeled appropriately (including serial number, Art Unit 2189, and type of response) and mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, hand-carried or delivered to the Customer Service Window at Randolph Building, 401 Dulany Street, Alexandria, VA 22313, or faxed to (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.



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